Listing of Claims

1. (Original) A method comprising:

partitioning state-sequenced information for communication to a computer subsystem;

communicating the partitioned information to the subsystem over a plurality of

input/output busses; and

separately processing partitioned information received over each of the plurality of

input/output busses, without first re-sequencing the information.

2. (Original) The method of claim 1, wherein the separately processing further

comprises obtaining state information from the received information, and processing the

information in a proper state context.

3. (Original) The method of claim 1, wherein the communicating partitioned

state-sequenced information comprises performing at least one direct memory access (DMA)

across each of the plurality of input/output busses.

4. (Original) The method of claim 1, wherein the communicating partitioned

state-sequenced information comprises communicating the information over a peripheral

component interface (PCI) bus.

5. (Original) The method of claim 1, wherein the information includes graphics

information and the separately processing comprises performing graphics processing on the

partitioned information.

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6.   (Original) The method of claim 1, wherein separately processing comprises performing an independent rendering on information received on each of the plurality of busses.

7.   (Currently amended) A computer system comprising:

a host processor configured to execute a single-threaded application;

partitioning logic for partitioning [[the]] state-sequenced information,

communication logic configured to communicate partitioned state-sequenced information across a plurality of input/output busses;

a plurality of interfaces located at a subsystem for receiving the information communicated across the plurality of the input/output busses;

processing logic for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed.

8.   (Original) The system of claim 7, further comprising a buffer memory in communication with the host processor for storing state-sequenced information for communication to a subsystem.

9.   (Original) The system of claim 7, wherein the processing logic is located at the subsystem.

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10.   (Original) The system of claim 7, wherein the partitioning logic is located in at the subsystem.

11.   (Original) The system of claim 7, wherein the partitioning logic is located in at the at the host processor.

12.   (Original) The system of claim 15, wherein the system is a computer graphics system.

13.   (Original) The system of claim 7, wherein the processing logic comprises at least one geometry accelerator.

14.   (Original) The system of claim 7, wherein each of the input/output busses are peripheral component interface (PCI) busses.

15.   (Original) The system of claim 7, wherein the system comprises a plurality of processing nodes that are coupled through a communication network.

16.   (Original) The system of claim 15, wherein the processing logic comprises work queues maintained among the processing nodes.

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